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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/025,165	12/19/2001	Jose L. Cervantes	10002896-1	6155

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EXAMINER	
SURYAWANSHI, SURESH	

ART UNIT	PAPER NUMBER
2115	

DATE MAILED: 10/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/025,165	CERVANTES, JOSE L.	
	Examiner	Art Unit	
	Suresh K. Suryawanshi	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 August 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24 and 28-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24 and 28-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment and Response dated 08/22/2005.

2. Claims 1-24 and newly added 28-31 are presented for examination.

3. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

4. The rejections are respectfully maintained and reproduced infra for applicant's convenience.

5. Claims 1-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bui (US Patent No 6,763,478 B1[1]) in view of Kelly (US Patent No 6,336,166 B1[1]).

6. As per claim 1, Bui discloses a portable computer having a first power mode and a second power mode, comprising:

a first memory bus [Fig. 1 and 2; col. 5, lines 3-13; memory bus 95];

[1] Prior art cited by examiner in the prior office action.

a control system coupled to the first memory bus, wherein the control system is configured to operate the first memory bus at a first speed in the first power mode, and a second speed different than the first speed in the second power mode [col. 5, lines 3-16, 30-32, 43-51; col. 6, lines 20-22, 52-54; col. 7, lines 8-9; col. 8, lines 13-15; a controller].

Bui does not expressly disclose about a second memory bus. However, Kelly clearly discloses about a computer system having a ROM bus and a RAM bus wherein buses are separate and independent of each other [Fig. 2; ROM and DRAM; col. 3, lines 22-30]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have more than one memory buses in a computer system and thereto controlling the speed of more than one memory buses accordingly. Moreover, clearly a system will save additional power by reducing the speed of more than one memory buses and a routineer will do so to extend the battery life of a portable computer when the portable computer is not operated via an external power source.

7. As per claims 11 and 17, Bui discloses a computer having a first battery power mode and a second external power mode, the computer comprising:

a random access memory [Fig. 1 and 2; SDRAM memory; col. 6, lines 58; RAM memory];

a first memory bus in communication with the random access memory [Fig. 1 and 2; memory bus 95];

a control system coupled to the first memory bus for reading and writing the random access memory, the control system including a clock generator, wherein the control system is configured to operate the first memory bus at a first clock speed in the first battery power mode, and a second clock speed greater than the first clock speed in the second power mode [col. 5, lines 3-16, 30-32, 43-51; col. 6, lines 20-22, 52-54; col. 7, lines 8-9; col. 8, lines 13-15; a controller].

Bui does not expressly disclose about a second memory bus. However, Kelly clearly discloses about a computer system having a ROM bus and a RAM bus wherein buses are separate and independent of each other [Fig. 2; ROM and DRAM; col. 3, lines 22-30]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have more than one memory buses in a computer system and thereto controlling the speed of more than one memory buses accordingly. Moreover, clearly a system will save additional power by reducing the speed of more than one memory buses and a routineer will do so to extend the battery life of a portable computer when the portable computer is not operated via an external power source.

8. As per claim 21, Bui discloses a method of managing power in a mobile computing device comprising:

determining whether the mobile computing device is operating in a first power mode or a second power mode [col. 1, line 62 -- col. 2, line 3; col. 4, lines 26-29];

operating a first memory bus at a first bus speed when the mobile computing device is in the first power mode [col. 5, lines 3-16, 30-32, 43-51; operating the memory bus at 66 MHz in the first power mode]; and

operating the first memory bus at a second bus speed different from the first bus speed when the mobile computing device is in the second power mode [col. 5, lines 3-16, 30-32, 43-51; operating the memory bus at 100 MHz in the second power mode].

Bui does not expressly disclose about a second memory bus. However, Kelly clearly discloses about a computer system having a ROM bus and a RAM bus wherein buses are separate and independent of each other [Fig. 2; ROM and DRAM; col. 3, lines 22-30]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have more than one memory buses in a computer system and thereto controlling the speed of more than one memory buses accordingly. Moreover, clearly a system will save additional power by reducing the speed of more than one memory buses and a routineer will do

so to extend the battery life of a portable computer when the portable computer is not operated via an external power source.

9. As per claims 2 and 24, Bui teaches that in the first power mode, the portable compute is operated via a battery power source, and in the second power mode the computer is operated via an external power source [col. 5, lines 3-16, 30-32, 43-51].

10. As per claims 3, 4 and 12, Bui teaches that a power mode detector which detects whether the portable computer is in the first power mode or the second power mode [col. 1, line 62 -- col. 2, line 3; col. 4, lines 26-29].

11. As per claims 5 and 13, Bui teaches that the second bus speed is double the first bus speed [col. 5, lines 3-13].

12. As per claim 6, Bui teaches that a clock generator [Fig. 2; col. 5, lines 3-5; clock generator].

13. As per claims 7 and 14, Bui teaches that a bus speed input for switching the portable computer between the first bus speed and the second bus speed [col. 5, lines 3-16, 30-32, 43-51].

14. As per claims 8 and 15, Bui teaches that the control system includes processor and a chipset [Fig. 1 and 2].

15. As per claims 9 and 16, Bui teaches that the memory bus is in communication with the chipset [Fig. 1 and 2].

16. As per claim 10, Bui teaches that an override switch coupled to the control system for switching the memory bus to the first speed or the second speed [col. 2, lines 4-11; user can override the default setting].

17. As per claims 18 and 19, Bui teaches that the mobile computing device is a laptop computer [col. 1, lines 10-13].

18. As per claim 22, Bui teaches that controlling a clock generator to determine the memory bus speed [Fig. 2; col. 5, lines 3-5; clock generator].

19. As per claim 23, Bui teaches that determining the memory bus speed independent of an internal processor bus speed [Fig. 2; col. 5, lines 3-51].

20. As per claim 28, Bui discloses a computer having a first battery power mode and a second external power mode, the device comprising:

a random access memory [Fig. 1 and 2; SDRAM memory; col. 6, lines 58; RAM memory];

a first memory bus in communication with the random access memory [Fig. 1 and 2; memory bus 95];

a control system coupled to the first memory bus for reading and writing the random access memory, the control system including a clock generator, wherein the control system is configured to operate the first memory bus at a first clock speed in the first battery power mode, and a second clock speed greater than the first clock speed in the second power mode [col. 5,

lines 3-16, 30-32, 43-51; col. 6, lines 20-22, 52-54; col. 7, lines 8-9; col. 8, lines 13-15; a controller]; and

a performance level input in communication with the control system for defining the first clock speed and the second clock speed [col. 2, lines 4-11].

Bui does not expressly disclose about a second memory bus. However, Kelly clearly discloses about a computer system having a ROM bus and a RAM bus wherein buses are separate and independent of each other [Fig. 2; ROM and DRAM; col. 3, lines 22-30]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have more than one memory buses in a computer system and thereto controlling the speed of more than one memory buses accordingly. Moreover, clearly a system will save additional power by reducing the speed of more than one memory buses and a routineer will do so to extend the battery life of a portable computer when the portable computer is not operated via an external power source.

21. As per claims 29-30, Bui discloses that users can manually adjust a mode of operation by accessing an applet [col. 2, lines 4-11]. Therefore, it would have been obvious to one of ordinary skill in the art to use a similar applet or modify the applet to provide the performance level input configuration.

Response to Arguments

22. Applicant's arguments filed August 22, 2005 have been fully considered but they are not persuasive.

23. In the remarks, applicant argued in substance that (1) Bui fails to disclose a second memory bus either alone or in view of Kelly; (2) Bui fails to disclose a control system that is configured to operate the memory busses at a first speed in the first power mode and a second speed different than the first speed in the second power mode.

24. As to point (1), Bui clearly discloses the invention for a plurality of busses [col. 3, lines 55-57; col. 3, line 65 -- col. 4, line 6; col. 5, lines 3-16]. Bui discloses the invention in view of two busses [the front side bus (FSB) 105 and the memory bus 95 as shown in Fig. 2]. Bui does not expressly disclose about a second memory bus. But a routineer in the art would know that it is very common in the modern computing devices having more than one memory bus (RAM bus and ROM bus). However, Kelly expressly discloses this [col. 3, lines 23-30; a computing system comprising of a ROM bus and RAM busses]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made that either the disclosed system of Bui had a secondary memory bus but not expressly disclosed or to combine the both cited references as both are related to busses. Moreover, Bui expressly discloses that the invention could be implemented for different bus architectures [col. 5, lines 52-67]. Thus, a routineer would easily

be able to expand the disclosed invention by Bui in view of Kelly not only for a plurality of different busses but also for two different memory busses.

25. As to point (2), Bui clearly discloses a controller that instructs the clock generator to generate appropriate clocks [col. 6, lines 20-22, 52-54; col. 7, lines 8-9; col. 8, lines 13-15].

Conclusion

26. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suresh K. Suryawanshi whose telephone number is 571-272-3668. The examiner can normally be reached on 9:00am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

sks
October 19, 2005